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Using Monte Carlo simulations, we study pseudomorphic uniformly doped AlGaAs/InGaAs/GaAs high electron mobility transistors with very short gate lengths (150 and 50 nm). In open-channel range of operation the saturation of the rain current is ensured by the existence of a pseudodipolar domain between the gate and the drain where the increase in drain potential is dropped. We describe the short channel effects, such as the high drain conductance, that occur in the pinchoff range of operation (especially in the shortest device). In this case the overheated electrons can easily transfer to the upper large band gap layer and cannot form any domain. The potential barrier that controls the current is gradually lowered by the drain potential increase, which is favoring the electron injection from the source side. Short channel effects are also involved in the relatively weak transconductance obtained in the 50 nm gate device, $g_m=800$ mS/mm, to be compared with 900 mS/mm reached in a 150 nm gate device. Finally, we show that the occurring of short channel effects can be predicted from very simple one-dimensional calculations along two perpendicular directions of the device, by taking into account the lateral diffusion from the source access zone to the active zone.

I. INTRODUCTION

Performance improvements of high electron mobility transistors (HEMTs) are mainly achieved by scaling down dimensions using high resolution electron beam lithography. Moreover, AlGaAs/InGaAs pseudomorphic HEMTs have shown better performances than the conventional AlGaAs/GaAs HEMTs, owing to better electron confinement within the channel and better transport properties in InGaAs.[1–4] At a given Al mole fraction in AlGaAs the pseudomorphic AlGaAs/InGaAs system provides a larger conduction band discontinuity than the conventional AlGaAs/GaAs system.[5] Thus, the use of a low Al concentration ($x_{Al}\leqslant 0.2$) in the pseudomorphic system allows, while keeping a high conduction band discontinuity, for the reduction of undesirable trapping effects due to deep donor centers such as persistent photoconductivity[6] or threshold voltage shift with temperature[7] that occur in conventional HEMTs. Trapping effects can also be reduced by using the very promising delta-doping technique in AlGaAs with higher Al content ($x_{Al}\geqslant 0.3$).[8] However for very short gate lengths, important shifts of threshold voltage[9] and severe deterioration of pinchoff characteristics occur due to short-channel effects.

In order to investigate the ultimate limitations in reducing the gate length, we have studied very short gate (50 and 150 nm) pseudomorphic InGaAs HEMTs using a particle ensemble Monte Carlo simulation. This modeling technique is the most accurate method for taking into account at the same time the bidimensional electrostatic potential, the nonstationary transport, and the real space transfer (RST) that are yet of prime importance in longer HEMTs.[10]

The geometry of the simulated devices and the ensemble Monte Carlo model are described in Sec. II A. The main macroscopic results and device performances are shortly presented in Sec. II B, before the physical analysis of device operation (Sec. II C) that constitutes the main feature of this study. We finally propose in Sec. III a very simplified but rapid method to obtain estimation of the importance of short-channel effects according to the semiconductor layer structure and the gate length to be used.

II. MONTE CARLO MODELING

A. The model

A typical basic structure of the device (Fig. 1) consists of an undoped GaAs buffer layer, on which are grown a nonintentionally doped 15-nm-thick strained $In_{0.2}Ga_{0.8}As$ layer (the channel), a 5-nm-thick spacer layer (undoped $Al_{0.2}Ga_{0.8}As$) and a N^+-doped AlGaAs layer ($N_D=2.10^{18}\times cm^{-3}$). In the simulations, the Schottky-barrier height Φ_B is assumed to be 0.75 V. The source and drain N^+ zones are doped to 2.10^{18} cm^{-3}. The contact depth in the GaAs buffer layer is 85 nm. It was recently proven that this parameter plays an important role in short-channel effects especially in self-aligned AlGaAs/GaAs HEMTs,[11] but our structure is not greatly affected by this effect: it is not self-aligned and the energy barrier between the channel and the substrate partially cancels the substrate leakage current. Two different gate lengths have been studied ($L_G=50$ nm in DEV50 and 150 nm in DEV150). In both cases, the source-gate distance L_{SG} is 0.1 μm and gate-drain distance L_{GD} is 0.5 μm. In the access zones (in other words the ungated ones) of a real device, the N^+-AlGaAs layer is made thick enough (about 40 nm) to reduce the

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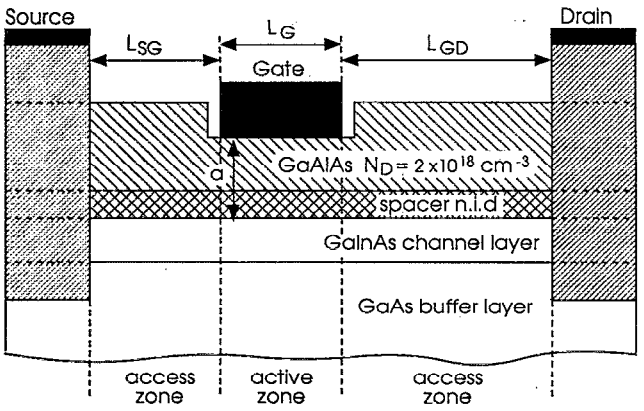

FIG. 1. Cross section of the basic structure used in the simulation.

access resistances to a minimum: thermal equilibrium is assumed to be recovered between the surface depletion due to trapping effects and the interface space charge layer. A GaAs added cap layer can also be deposited in order to "passivate" the surface. In this work, neither cap layer nor surface trapping effects are taken into account and the N^+-AlGaAs thickness has been reduced to 25 nm, which is sufficient to get low access resistance in this layer while minimizing the number of simulated particles.

Short channel effects such as the shift of threshold voltage in subquarter-micrometer HEMTs and MESFETs are related to the low value of the aspect ratio (L_G/a),[9,12] where a is the total AlGaAs layer thickness in the gated region. But in the case of a 50 nm gate length, an aspect ratio greater than 5 (that is the minimum value required to prevent the shift of V_T) leads to a thickness $a=10$ nm, including the spacer layer. Consequently, problems of tunneling between the channel and the gate could appear and the doping level in the top layer should be as high as 10^{19} cm^{-3} in order to obtain a reasonable gate voltage range of operation. Then we considered more realistic structures where the aspect ratio was 2.27 (in DEV50) and 5 (in DEV150).

The 2DG (2-dimensional in geometrical space) particle Monte Carlo technique for device modeling allows us to take into account the nonstationary carrier transport as well as any two-dimensional device geometry. Our model has been described in detail elsewhere.[13] Vertical as well as horizontal rectangular meshing for Poisson's equation solution can be varied in the simulated device, according to local geometrical and doping parameters, in order to ensure that the cell dimensions are smaller than the Debye length in every zone of the device. The time step Δt_p between two updates of the electric field is taken to be 1 fs, which is inferior to the smallest dielectric relaxation time in the highest doped zone of the device (up to 2×10^{18} cm^{-3} in this work) and to the inverse of the plasma frequency. This ensures that the system can relax after every local perturbation, without errors due to the "frozen" local field. For solving the Poisson equation, the impurities are assumed to be fully ionized. Neither degeneracy effects nor electron-electron scattering is taken into account in this model.

There is no notion of fixed time step for the calculation of electron motion: the free-flight time t_f is determined from scattering frequencies. An electron is always accelerated by the real local electric field as every crossing of a cell boundary is detected during each free flight; after crossing a cell boundary, the motion is broken off and is continued taking into account the field of the new cell. This caution is of the utmost importance for the simulation of very short devices, since the electric field gradient may be very strong and the electron transport is mainly ballistic or quasi-ballistic in the active zone.

At every metal-semiconductor interface the boundary conditions fix the electrostatic potential, and in the cells adjacent to the ohmic contacts the equilibrium electron concentration is assumed to be recovered $(n=N_D)$. This last boundary condition is thus the condition of carrier injection, whose initial energy and momentum are specified by a Maxwellian distribution. At free surfaces the normal component of the electric field is assumed to be zero. A large number of particles, typically here 24 000, is initially implanted in the device.

Band structure and main scattering parameters in strained InGaAs such as the effective mass m^* in Γ valley, the energy of polar optical phonon $\hbar\omega_0$ and the conduction band discontinuity ΔE_c with AlGaAs are taken from relevant experimental measurements reported in the literature.[5,14,15] Other parameters that are not available from experimental measurements were extrapolated from well known bulk material parameters. Using these data in the Monte Carlo program, the steady-state velocity-field characteristic was calculated in a uniform electric field and exhibited a low field mobility $\mu=9000$ cm^2 V^{-1} s^{-1} and a peak velocity $v_p=2.3\times10^7$ cm/s.

Finally, it is worth noting that the two-dimensional quantization of electron energy states in the quantum well is not accounted for in our 2DG program: the low-field carrier velocity is not greatly affected by such a simplification, at least at room temperature, as was shown both experimentally and theoretically.[16–18]

B. Drain characteristics and device performance

Figure 2 shows the drain current characteristics $I_D(V_{DS})$ obtained for each simulated device. At high gate bias voltages, i.e., in open-channel range of operation, a rather good saturation of the drain current is observed in both devices as soon as the drain voltage reaches about 0.5 V.

At low V_{GS}, i.e., in pinchoff range of operation, the drain current increases almost exponentially with V_{DS} and seems to saturate only at high V_{DS}. This results in a high drain conductance g_D, which is detrimental for high frequency applications due to the decrease of maximum oscillation frequency, and for logic operation due to the imprecise definition of the low state logical level. This phenomenon is especially obvious in the shortest device (DEV50) and is considered as a short-channel effect.

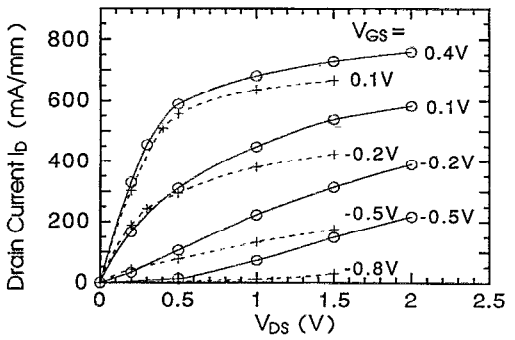

FIG. 2. Drain current-voltage characteristics of DEV50 (circles, solid lines) and DEV150 (cross, dashed lines).

It should be noted that to obtain about the same threshold voltage in both devices despite this short-channel effect, the total thickness of AlGaAs in the gated region has been reduced in the shortest device (22 nm instead of 30 nm). This results in a higher current level in the 50 nm gate transistor than in the 150 nm gate one for a specific set of gate and drain voltages.

As it is usually done, the threshold voltages V_T have been extrapolated from $\sqrt{I_D}$ vs V_{GS} curves for a given drain voltage. They have been compared with the theoretical value V_{FB} of the flat-band voltage that is given by the classical formula:

$$V_{FB}=\Phi_B-\Delta E_c-V_{P2}-\xi_1,$$

where Φ_B is the surface Schottky barrier height, ΔE_c is the conduction band discontinuity between channel and large band gap material, V_{P2} is the pinchoff voltage of the highly doped AlGaAs material, and ξ_1 is the energy difference between the conduction band and the Fermi level in the channel material at thermal equilibrium. Although V_{FB} is never exactly equal to the threshold voltage even for a long gate device, we defined the threshold voltage shift as $\Delta V_T = V_{FB}-V_T$. Values of V_{FB} and ΔV_T ar reported in Table I for each device and for different drain voltages. Values obtained for two other devices with different aspect ratio are also reported. As it is usually expected in short gate length field-effect transistors (FETs), ΔV_T is all the greater and its dependence on V_{DS} is all the stronger as the aspect ratio is smaller.

The transconductance performances show evidence for another aspect of short-channel effects. The transconductance is calculated as the slope of the drain current versus the gate voltage at a fixed drain voltage: $g_m=(\partial I_D/\partial V_{GS})V_{DS}$. The maximum transconductance g_{mmax}, calculated at $V_{DS}=1$ V, is not improved and even becomes worse as the gate length is reduced from 150 nm (900 mS/mm) to 50 nm (790 mS/mm).

The total gate capacitance $C_{GS}+C_{GD}$ can be calculated by the derivation of the total charge present in the device, with respect to the gate voltage at a given drain voltage. This calculation is underestimating the capacitances since it does not take into account the parasitic capacitances due to access lines nor the capacitance between the gate and the edge of the real recess profile. These added capacitances do not depend on the gate length and are not always negligible by comparison with the gate to channel capacitance that becomes very low in such short devices. Keeping these restrictions in mind, we have calculated f_T as $g_m/2\pi(C_{GS}+C_{GD})$. That yields therefore an overestimation of f_T compared with a real device, but, as recently shown,[19] it is a perfectly valid calculation of the current gain cutoff frequency of this intrinsic simulated device. Despite the decrease in transconductance, the transition frequency f_T increases as the gate length is reduced (360 GHz in DEV50 instead of 250 GHz in DEV150). This improvement is due to the decrease of the calculated gate capacitance.

C. Analysis of very short device operation

In this section, we describe the physical phenomena involved in the very short device operation, namely the drain current saturation and the blocking mechanisms at different gate bias voltages.

1. Nonstationary transport

In devices with such short active zones, electron transport is highly nonstationary: most electrons are traveling through the gate-controlled zone (where the longitudinal electric field is high) without suffering any scattering (or very few inefficient scatterings such as the emission of a polar optical phonon). Under these conditions of ballistic or quasi-ballistic transport, they can reach very high drift velocities, much higher than stationary ones.

To show up the nonstationary nature of electron transport in the active zone and to get a quantitative comparison between DEV50 and DEV150, we studied the device operation at a drain bias of 1.0 V and a gate bias that corresponds in each case to the maximum transconductance ($V_{GS}=0.1$ V for DEV50 and $V_{GS}=-0.2$ V for DEV150).

TABLE I. Threshold voltages V_T and threshold voltage shifts ΔV_T for DEV150, DEV50, and two other devices with (a) $L_G=150$ nm and (b) $L_G=100$ nm.

			$V_{DS}=1$ V		$V_{DS}=1.5$ V	
Device	L_G/a	V_{FB}(V)	V_T(V)	ΔV_T(V)	V_T(V)	ΔV_T(V)
(a)	6	−0.25	−0.52	0.27		
DEV150	5	−0.57	−0.92	0.35	−1.04	0.47
(b)	4.6	−0.1	−0.42	0.32	−0.55	0.45
DEV50	2.3	−0.1	−0.9	0.8	−1.2	1.1

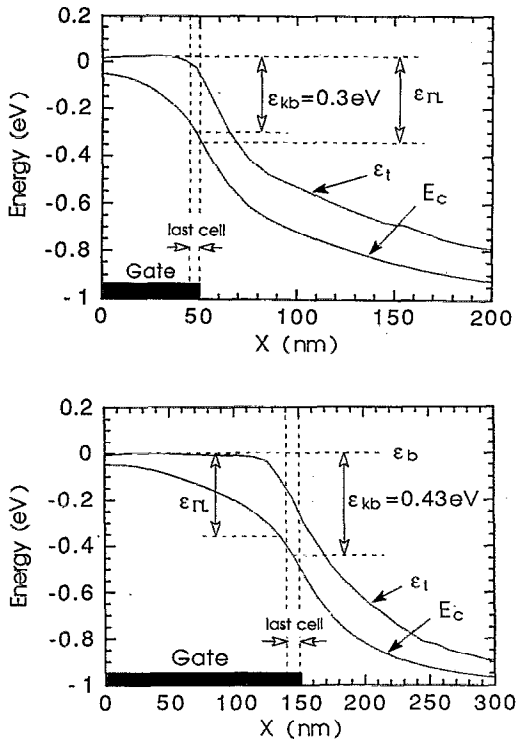

FIG. 3. Bottom of conduction band (ϵ_c) and average total energy of electrons ($\epsilon_t = E_c + \epsilon_k$) as a function of distance along the channel at a drain bias of 1 V. The gate bias corresponds to the maximum transconductance. ϵ_{kb} is the average kinetic energy of ballistic electrons in the last cell under the gate, i.e., the region where the spectra of kinetic energies of Fig. 4 are taken. (a) DEV50, $V_{GS}=0.1$ V. (b) DEV150, $V_{GS}=-0.2$ V.

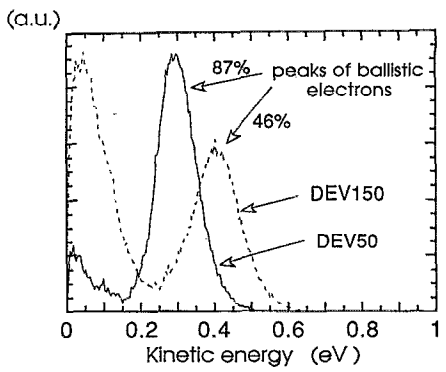

FIG. 4. Distribution of kinetic energies in the last cell of the channel under the gate for $V_{DS}=1$ V with mention of ballistic electrons ratio. The gate bias corresponds to the maximum transconductance ($V_{GS}=0.1$ V for DEV50, $V_{GS}=-0.2$ V for DEV150).

In Fig. 3(a) the profile of the bottom of the conduction band E_c (Γ valley) is plotted for DEV50 along the channel together with the average "total" energy ϵ_t of the electrons. The difference $\epsilon_t - E_c$ between the two curves yields the average kinetic energy ϵ_k of the electron population (i.e., in the case of K space transferred electrons, $\epsilon_{\Gamma L}$ and $\epsilon_{\Gamma X}$ are not included in ϵ_t). The main point is that the total energy is nearly constant under the gate: electrons do not lose any energy through lattice scattering under the gate. This is typical of ballistic or at least quasi-ballistic transport. This is confirmed in Fig. 4 where we have plotted (in solid line) the distribution of particle kinetic energies located in the last cells of the gate-controlled channel [between $x=45$ nm and $x=50$ nm in Fig. 3(a)]. This distribution exhibits a peak centered on 0.3 eV that is the average kinetic energy ϵ_{kb} of purely ballistic electrons as shown in Fig. 3(a). Thus, this peak corresponds to the "ballistic" population in these cells. Since the kinetic energy ϵ_{kb} is less than the Γ-L separation ($\epsilon_{\Gamma L}=0.36$ eV) the k space transfer can only occur after the gate end so that the population contained in the "ballistic peak" represents 87% of the total population and supplies 96% of the current through this cross section.

The same figures are plotted again for DEV150 [Figs. 3(b) and 4 (dashed line)]. In this case the total energy is nearly constant along most part of the gate but decreases significantly (25 nm) before the end of the gate. In the last cell located under the gate [between $x=140$ nm and $x=150$ nm in Fig. 3(b)] the kinetic energy ϵ_{kb} of purely ballistic electrons would be 0.43 eV and the distribution of particle kinetic energies counted in the same cell exhibits a peak centered on about the same value. As opposed to the previous case, this kinetic energy is greater than $\epsilon_{\Gamma L}$ so that the k space transfer, which randomizes the direction of the velocities, can be significant before the gate end. It is responsible for the decrease in the average kinetic energy and then the total energy. Indeed the ballistic peak represents here only 47% of the total population. Some important quantitative results are summed up in Table II.

The gate reduction from 150 nm down to 50 nm increases the velocity under the gate: a maximum drift velocity overshoot as high as 9×10^7 cm/s is reached in DEV50 instead of 8×10^7 cm/s in DEV150. This should lead to very short transit time, that is to say very high transition frequency, but this is not sufficient to improve the transconductance. As described in the next paragraphs, the efficiency of the current control by the gate-source voltage is disturbed by a detrimental influence of drain voltage.

2. Open channel range of operation ($V_{GS}=0.4$ V) for $L_G=50$ nm

At this gate voltage the drain current is well saturated. The saturation of the drain current generally requires the existence of two zones in the channel between source and drain: a gate-controlled zone along which is dropped the saturation drain voltage V_{Dsat} and a space charge layer (SCL) which supports any further increase of bias drain voltage. The SCL acts as a screen for the active zone

TABLE II. Ballistic transport and velocity overshoot in both devices (for $V_{DS}=1.0$ V and for V_{GS} corresponding to the maximum of g_m). (a) In the channel, just at the end of the gate; (b) parallel to the channel.

L_G (nm)	% of ballistic electrons in the population (a)	% of current due to ballistic electrons (a)	Maximum drift velocity (b)
150	46%	79%	8×10^7 cm/s
50	87%	96%	9×10^7 cm/s

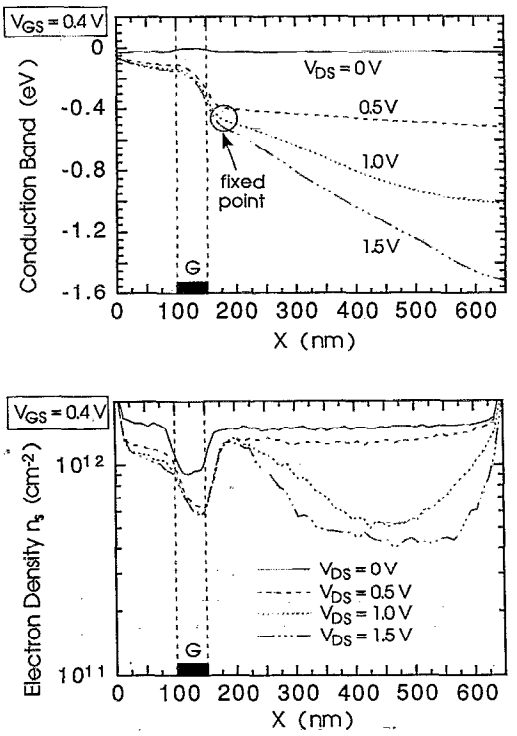

FIG. 5. Influence of V_{DS} in open-channel operation (DEV50, V_{GS}=0.4 V). (a) Bottom of conduction band and (b) channel electron density as a function of distance along the channel.

against the variations of drain voltage: the conditions of electron injection in the active zone become independent on V_{DS}.

This effect is shown in Fig. 5(a) where we have plotted the profile of the bottom of the conduction band along the channel between the two heavily doped zones of source and drain contacts, for different drain voltages ranging from 0 to 1.5 V. Beyond the onset of saturation ($V_{DS}\geqslant$0.5 V), the conduction band is nearly fixed at the end of the gate [see the "fixed point" in Fig. 5(a)] and the excess drain voltage is dropped between the fixed point and the drain.

The profile of the channel electron density versus the distance between source and drain is plotted in Fig. 5(b) at different drain voltages. Before saturation ($V_{DS}<$0.5 V), and increase in V_{DS} tends to deplete the active zone without inducing any channel pinchoff near the drain edge of the gate (the perpendicular electric field remains still confining). Beyond the onset of saturation ($V_{DS}\geqslant$0.5 V), the electron density in the active zone becomes nearly independent on the drain voltage; this is consistent with the conduction band profiles in Fig. 5(a).

Since most electrons cross the active zone ballistically, their momentum is parallel to the interface and they cannot easily transfer to the high band gap material. But as soon as they have a sufficient energy ($\epsilon_{\Gamma L}$=0.36 eV), they have a greater probability of transferring in the lateral valleys and then for initiating the arising of an accumulation of slow electrons in the main channel, as shown in Fig. 6, which is a plot of the spatial distribution of particles in the

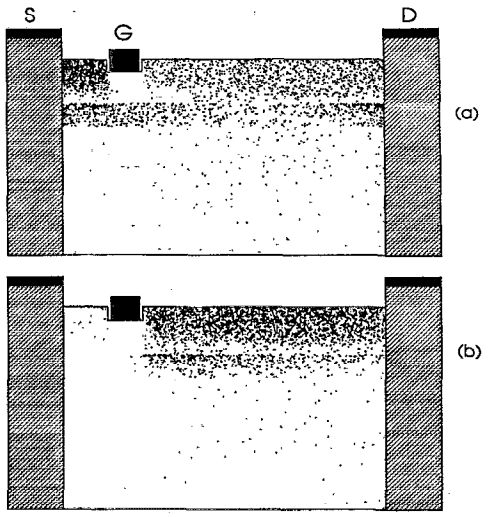

FIG. 6. Electron reparation for V_{DS}=1 V in open-channel operation (DEV50, V_{GS}=0.4 V). (a) Γ valley; (b) L and X valleys.

device at V_{DS}=1 V (i.e., corresponding to a saturated drain current). This accumulation is followed by a depleted zone where the electrons are accelerated by the electric field and part of them is transferred little by little to the high band gap material. The entity "accumulation-depletion" SCL constitutes a kind of dipolar domain, where the increase in excess drain voltage is dropped. This screening mechanism ensures a good electron flow control under the gate: for V_{DS} ranging between 1 and 1.5 V, the channel electron density does not change and the peak velocity only increases by 7%, as does the drain current. Moreover, the conduction band discontinuity between the channel and the GaAs buffer layer ensures a good confinement of the electron gas so the leakage current through the buffer is weak. It becomes significant (not more than 12% of total drain current) only behind the accumulation of k space transferred electrons.

3. Pinchoff range of operation ($V_{GS}=-0.2$ V) for L_G=50 nm

In this case, the perpendicular electric field component is no more confining and the channel is theoretically pinched off.

The evolution of the conduction band along the channel between source and drain is plotted in Fig. 7(a). The difference with the previous case [V_{GS}=0.4 V, Fig. 5(a)] is clear: there is no "fixed point" and the whole drain voltage is applied across the active zone that is to say the longitudinal component of the electric field goes on increasing dramatically as V_{DS} does. At this gate voltage, the current is controlled by a potential barrier that prevents the electron diffusion from the source side. This barrier is modulated by variations of drain potential [as shown in Fig. 7(a)] and the current increases as and when the barrier is decreased.

It is again well confirmed by the evolution of the electron density along the channel between source and drain that is plotted in Fig 7(b) at different drain voltages. As

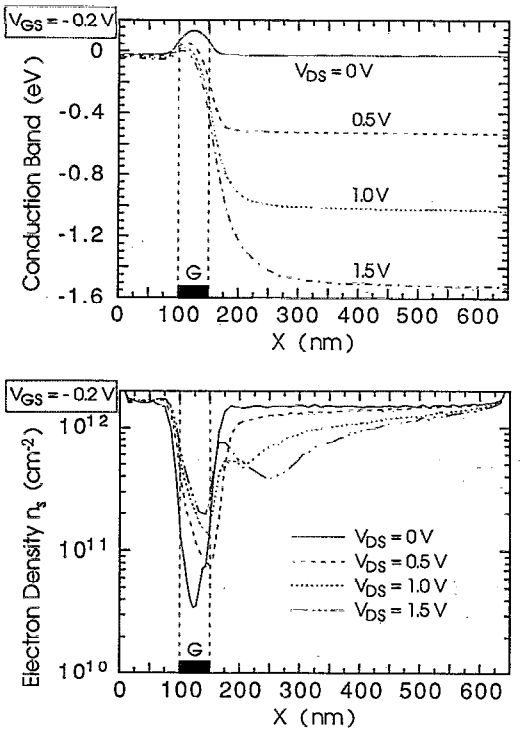

FIG. 7. Influence of V_{DS} in pinchoff operation (DEV50, $V_{GS}=-0.2$ V). (a) Bottom of conduction band and (b) channel electron density as a function of distance along the channel.

opposed to the previous case ($V_{GS}=0.4$ V), the electron density in the active zone increases a great deal by diffusion from the source side as drain voltage is increased. This situation is similar to what was found in a permeable base transistor[20] where the drain characteristics are damaged by the so-called "drain induced barrier lowering" effect.

In these bias conditions, the electric field is very strong in the active zone. Since most electrons cross this zone ballistically, they may gain before suffering any scattering an energy much higher than the threshold energy necessary to transfer either in the lateral valleys of InGaAs ($\epsilon_{\Gamma L}=0.36$ eV and $\epsilon_{\Gamma X}=0.55$ eV) or in the upper AlGaAs layer ($\Delta E_c=0.29$ eV). Consequently, electrons may easily transfer spatially towards the high band gap material immediately at the gate end: first transfer to InGaAs lateral valleys and then, after randomization of the velocity directions and owing to the perpendicular electric field, transfer to AlGaAs.[21] The particle distribution inside the device at $V_{DS}=1$ V is plotted in Fig. 8. Through a plane located 50 nm after the gate end (this plane is represented by a dashed arrow in Fig. 8), 60% of the drain current is supplied by electrons from the AlGaAs upper layer. The k space transferred electrons that so easily escape from the InGaAs channel cannot induce the arising of a trapped dipolar domain. Furthermore the electric field in the drain access zone is too low to accelerate electrons and create a depletion zone in the main channel. Figures 7(b) and 8 clearly show the absence in the channel of the "accumulation-depletion" SCL that has been described in the previous case of open-channel range of operation.

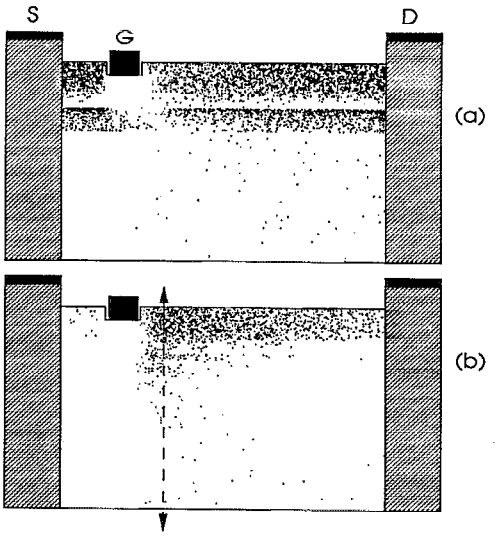

FIG. 8. Electron reparation for $V_{DS}=1$ V in pinchoff operation (DEV50, $V_{GS}=-0.2$ V). (a) Γ valley; (b) L and X valleys.

D. Gate voltage range of good operation

For each device, variations of main channel electron density n_s are plotted versus gate source voltage V_{GS} in Figs. 9(a) (DEV50) and 9(b) (DEV150), for different drain-source voltages from Monte Carlo simulations. The evolution of electron density in the parasitic channel arising in the high band gap material for high gate-source

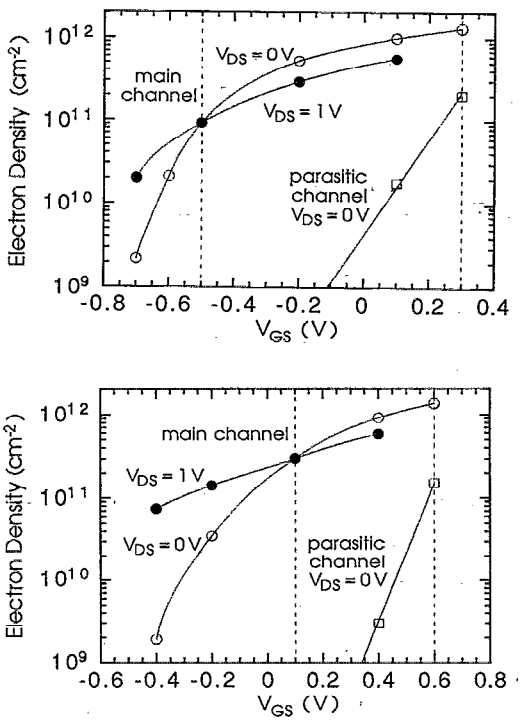

FIG. 9. Minimum electron density in the channel layer (circles) and in the GaAlAs layer (squares) as a function of gate voltage. The dashed lines hold for the gate voltage range of good device operation ΔV_{GS}. (a) DEV150; (b) DEV50.

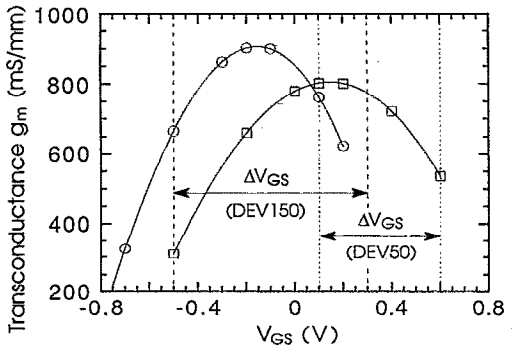

FIG. 10. Transconductance as a function of gate voltage for $V_{DS}=1$ V (solid lines). DEV150: circles; DEV50: squares. The range ΔV_{GS} is also reported (dashed lines).

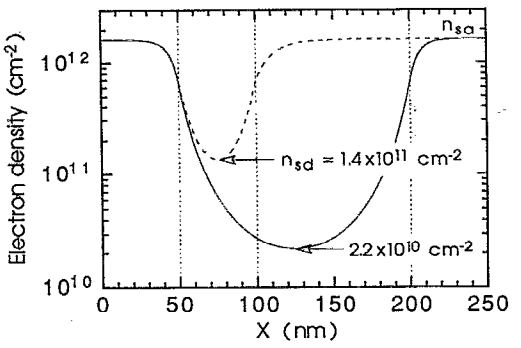

FIG. 11. Electron density profile calculated in an unbiased N^+NN^+ structure for two different lengths L of the N region. n_{sa} is the electron density in the access zones of the HEMT. n_{sd} is the resulting minimum density in the N region. $L=50$ nm: dashed line. $L=150$ nm: solid line.

voltages is also plotted in the same figures. From these curves, we can define the superior limit V_{sup} of gate voltage range ΔV_{GS} for good device operation when the electron density in parasitic channel becomes greater than about one tenth of the main channel density n_s. This criterion leads to $V_{sup}\approx 0.3$ V in DEV150 and $V_{sup}\approx 0.6$ V in DEV50. As previously seen, a good drain current control exists if n_s does not increase as V_{DS} is increased: this is the case only at high V_{GS}. For negative values of V_{GS}, namely under the intersection between the two curves in both Figs. 9(a) and 9(b), n_s increases greatly as V_{GS} increases because of electron injection due to the barrier lowering. This intersection point gives an estimation of the inferior limit V_{inf} of gate voltage range for good device operation (about -0.5 V for DEV150 and 0.1 V for DEV50).

In Fig. 10 is plotted the evolution of the transconductance g_m versus the gate voltage for both devices DEV150 and DEV50, submitted to a 1 V drain voltage. The gate voltage range $\Delta V_{GS}=V_{sup}-V_{inf}$ previously determined is reported for each curve. In the case of DEV150, maximum transconductance stands approximately in the middle of the range, whereas it stands very near the edge in the case of DEV50: electron diffusion from the source side still influences device operation for V_{GS} corresponding to the maximum transconductance and is then responsible for its relatively low value in the very small device.

III. SIMPLIFIED DOUBLE 1D STATIC ANALYSIS

We have tried to connect the problems of current control of the current shown by Monte Carlo modeling to a very simple but helpful 1DG calculation along both directions in the device. The 1DG Poisson's equation is solved self-consistently with the Fermi–Dirac statistics for carriers so that no current can be considered. Along the channel (i.e., in a direction parallel to the interfaces) this calculation can be made only at a 0 V drain voltage, and in a normal direction the simulation is only valid at gate voltages for which the gate current may be neglected.

A. 1D analysis along the channel (at $V_{DS}=0$ V)—Influence of lateral diffusion

By considering the HEMT structure at a 0 V drain voltage, the channel may be compared to a N^+NN^+ structure at thermal equilibrium where:

(i) the N region is the active zone of the transistor whose length is assumed to be the gate length.

(ii) the N^+ regions are the source and drain access zones.

In the access zones, the electron density n_{sa} in the InGaAs channel is determined at thermal equilibrium by the donor doping level N_D in the high band gap material (AlGaAs), together with the energy band discontinuity ΔE_c between the conduction bands of both materials constituting the heterojunction. In the active zone, at normal operation, the electron channel density n_s should be determined only by the gate voltage V_G whatever the gate length. But the difference of electron density between a N^+ region and an N one is relaxed over a few Debye lengths L_D whose value varies as the universe of the square root of the electron concentration (e.g., in InGaAs, $L_D\approx 160$ nm for $n=10^{15}$ cm^{-3}). Therefore, in a nanometric device where the gate length may be in the same order of magnitude as the Debye length, electron diffusion from access zone to active zone may influence the gate control of the charge, especially near the pinchoff.

In order to calculate the contribution of the diffusion according to the gate length and regardless of the gate effect, we have performed a 1D static simulation (i.e., solution of Poisson's equation) of nonbiased N^+NN^+ structures where the low doping level in the active N zone of length L is that of the unintentionally doped InGaAs layer (10^{15} cm^{-3}) and the high doping level of N^+ zones is derived from the electron density n_{sa} in the access zones. n_{sa} is calculated through the solution of Poisson's equation in a direction perpendicular to the layers ($n_{sa}=1.6\times 10^{12}$ cm^{-2}). We have plotted in Fig. 11 the electron density profile along the 1D structure for two N zones of different lengths L. For $L=150$ nm, n_s decreases down to 2.2×10^{10} cm^{-2}, whereas in the 50-nm-long structure it remains as

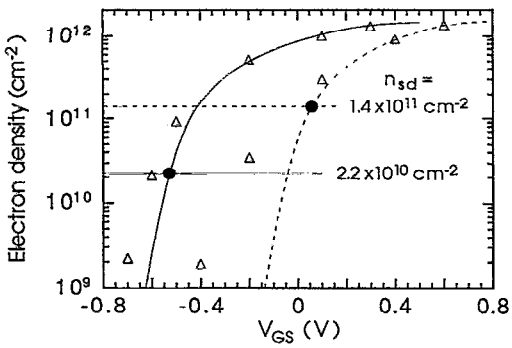

FIG. 12. Channel electron density calculated as a function of gate voltage using a simple 1DG model, in devices with two different active zone lengths (50 nm: dashed line, and 150 nm: solid line). Dots obtained from 2DG Monte Carlo simulations are reported for comparison, as well as previously calculated n_{sd} values.

high as about 1.4×10^{11} cm^{-2}. Let us call n_{sd} the minimum electron density obtained in the N^+NN^+ structure. If the N zone length L is too short, n_{sd} cannot reach the equilibrium value corresponding to the doping level (i.e., 1.5×10^{9} cm^{-2}) in the low doped N zone. For the shortest device, n_{sd} is ten times larger than it should be without the edge effect of lateral diffusion. This phenomenon highly influences the channel density control as it is shown in the following subsection.

B. 1D analysis of the charge control by the gate—Gate voltage range of good operation

The same simple 1D model may be used in the direction normal to the interfaces to study the gate effect on the channel electron density; the edge effect of lateral diffusion is then ignored.

In Fig. 12, the $n_s(V_G)$ curves obtained from the 1D Poisson equation resolution are plotted for two different AlGaAs layer thicknesses corresponding to both simulated devices (DEV50 and DEV150). In each case, the lowest channel density n_{sd} previously obtained in the associated N^+NN^+ structure is drawn, as well as for comparison, the dots corresponding to the channel electron density obtained from 2D Monte Carlo simulations at $V_{DS}=0$ V.

The gate voltage V_{inf} for which the curve $n_s(V_G)$ passes through the value n_{sd} gives an inferior limit of the range of good operation. This criterion leads to $V_{inf}=-0.53$ V for DEV150 and $V_{inf}=-0.06$ V for DEV50. As $n_s(V_G)$ is greater than n_{sd}, the lateral diffusion has only a weak influence on the total electron density and the gate efficiently controls the channel. On the contrary, as $n_s(V_G)$ is less than n_{sd}, the contribution of the diffusion begins to influence the channel control and makes the device pinch-off difficult. Indeed, this is well confirmed by the Monte Carlo dots (calculated at $V_{DS}=0$ V) that represent the resulting effect of gate voltage and lateral diffusion on the electron channel density: in the so-defined range of good operation ($V_{GS}>V_{inf}$), the dots agree very well with the $n_s(V_G)$ curve, whereas outside this range, they deviate significantly from the curve as and when the gate voltage is further decreased. This discrepancy at low V_G is all the greater as the gate length is shorter (i.e., the aspect ratio is smaller). Moreover, as it is greater (i.e., as the contribution of the diffusion is more important), n_s should be all the more sensitive to the drain voltage, as in a N^+NN^+ structure. Indeed for gate voltages lower than V_{inf} the drain current characteristics are badly saturated or badly pinched-off as previously seen in Fig. 2.

It is worth noting that the so obtained values of inferior limit V_{inf} are in good agreement with those previously determined from Monte Carlo calculations. This simple approach is sufficient to explain, in terms of diffusion, the detrimental short-channel effects that appear near the pinchoff and it yields a rather simple and rapid way to foretell the gate voltage range of good operation, according to the gate length and to the aspect ratio.

IV. CONCLUSION

Pseudomorphic HEMTs with nanometric gate lengths have been studied in order to investigate the physical phenomenon responsible for device performance limitations at ultrashort dimensions. Related to a weak aspect ratio, the main limiting factor is shown to be the bad drain current pinchoff due to electron lateral diffusion in the active zone, under the influence of the drain voltage. It induces high drain conductances as well as a relatively low maximum transconductance for a 50-nm-long gate device. At high gate voltages the drain characteristics are rather well saturated because of the arising of a pseudodipolar domain between the gate and the drain. Intrinsic frequency performances are not greatly affected by this short channel effect. The influence of nonstationary electron transport as well as real space transfer has been studied. From simple 1D diffusion considerations, we propose a rapid and efficient way to predict the gate voltage range for good device operation as a function of gate length and aspect ratio.

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